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Charge Transport Optimisation in Crystalline Silicon Photovoltaic Systems: Design, Fabrication, and Experimental Evaluation of a 60 A Maximum Power Point Tracking Charge Controller

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ABSTRACT
Photovoltaic energy conversion in crystalline silicon is governed by the nonlinear carrier transport properties of the p–n junction, whose current–voltage characteristic exhibits a distinct maximum power point (MPP) that shifts continuously with irradiance and junction temperature. Conventional pulse-width-modulation controllers cannot follow it and forfeit 20–30% of available energy. Well-characterised medium-to-high-current maximum power point tracking (MPPT) controllers designed for local fabrication are absent from the Nigerian technical literature; this work addresses that gap. A 60 A MPPT charge controller built on an asynchronous buck converter topology was designed, fabricated and evaluated. A Perturb and Observe algorithm runs on an Arduino Mega 2560, current is sensed through Hall-effect transducers that galvanically isolate the control stage from the power path, and five protection mechanisms guard against overvoltage, overcurrent, short circuit, reverse polarity and thermal runaway. Laboratory characterisation with a programmable PV-array emulator over 200–1000 W m^{-2} yielded a peak power conversion efficiency of 95.8%, a peak MPPT tracking efficiency of 98.2% and an output voltage ripple of 0.67%, with a maximum MOSFET junction temperature of 76 °C at the rated 60 A load. Outdoor testing over five clear-sky days using two 250 W_p monocrystalline panels in series returned average conversion and tracking efficiencies of 94.8% and 97.5%. Every design decision is traced to its condensed matter basis. The results establish that locally fabricated controllers built from commercially available semiconductor components can match imported commercial units, lowering the cost barrier to off-grid photovoltaic deployment in sub-Saharan Africa.

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INTRODUCTION

In crystalline silicon, solar energy conversion is essentially a quantum mechanical phenomenon: incoming photons with energies higher than the silicon bandgap ($E_g \approx 1.12$ eV) produce electron-hole pairs, which are then spatially separated by a p-n junction's inherent electric field (Villalva et al., 2009). On top of the typical diode dark-current characteristic, this carrier production generates a short-circuit current I_{sc} proportional to the incoming photon flux at the macroscopic level. The resulting terminal I-V curve is inherently nonlinear, with a distinct power maximum P = VI at a voltage V_{mpp} at the curve's knee, when current and voltage simultaneously reach significant levels (Batzelis et al., 2021). The Maximum Power Point (MPP) is defined by these criteria.

The fact that V_{mpp} is not a set amount is a major practical challenge. The open-circuit voltage is logarithmic to rising irradiance, whereas the photocurrent increases in a near-linear fashion, driving the MPP towards higher power and a slight increase in voltage. Increased junction temperature also decreases the semiconductor bandgap and increases the intrinsic carrier density, leading to a decrease in net output power by approximately –0.5% $°C^{-1}$ from Standard Test Conditions and a decrease in V_{oc}, at approximately –2.3 mV $°C^{-1}$ per silicon series cell, (Skoplaki & Palyvos, 2009). Nigeria is a tropical country with mean daily global horizontal irradiance that varies

by climatic zone from 4 to 7 kWh m^{-2} day^{-1} (Eweka et al., 2022). These combined effects result in a greatly changed MPP location throughout the day and intelligent real time tracking is now a practical and not an option requirement.

Conventional Pulse-Width Modulation (PWM) charge controllers regulate the charging of the battery, keeping the operational voltage of the solar array at or near the battery terminal voltage. Such a setup will also waste 20-30% of incident solar energy when irradiance changes due to the fact that battery voltage typically does not reach V_{mpp} (Faranda & Leva, 2008). MPPT controllers can eliminate this limitation by using a DC–DC converter that pulls the voltage of the array from the battery voltage, allowing the array to operate at its maximum power point all of the time. Perturb and Observe (P&O) is one of the widely used algorithms for tracking due to its low processing requirement, easy digital implementation and reasonable tracking accuracy under real irradiance profiles (Huynh & Dunnigan, 2016; Subudhi & Pradhan, 2013; Motahhir et al., 2021). If the PV array voltage is frequently higher than the battery voltage, a step-down (buck) converter is the obvious choice of DC-DC converter since it works by reducing the input voltage to match the output voltage. When the PV array is connected to multiple modules in series to reduce cable losses (Mohan et al., 2003), the higher input voltage makes it a step-down converter.

Although Nigeria has the largest economy in Africa and considerable solar energy, they still suffer from high grid energy deficits, which can be attributed to the ageing infrastructure and persistent shortage in installed generating capacity (World Bank, 2022). Solar photovoltaic mini-grids are the best approach to reduce energy poverty in underprivileged areas, according to the Rural Electrification Agency (2023). In light of this, locally manufactured, reasonably priced MPPT charge controllers are an essential enabling technology. Recent Nigerian photovoltaic research has, however, concentrated largely on array sizing and techno-economic assessment rather than on the power-conversion stage itself (Isa et al., 2026), leaving the controller hardware comparatively unexamined. The lack of a well-characterised medium-to-high current (60 A) MPPT controller intended for local manufacture from commercially accessible components is a reported gap in the Nigerian technical literature that the current effort fills. Condensed matter transport physics and the subsequent hardware design decisions are explicitly linked throughout the study.

Semiconductor Physics Background

Photovoltaic I–V Characteristics and the MPP

The electrical behaviour of a photovoltaic cell is well described by the single-diode equivalent circuit, which gives:

$$I = I_{ph} - I_0 \left\{ \exp\left[\frac{V+IR_s}{nV_T}\right] - 1 \right\} - \frac{(V+IR_s)}{R_{sh}} \qquad (1)$$

where I_{ph} is the photogenerated current (proportional to irradiance G), I_0 is the reverse saturation current (thermally activated), n is the diode ideality factor ($1 \leq n \leq 2$), $V_T = k_B\, T/q \approx 25.7$ mV at 298 K is the thermal voltage, R_s is series resistance, and R_{sh} is shunt resistance (Batzelis et al., 2021). At the MPP, the condition $\partial P/\partial V = 0$ reduces to:

$$I_{mpp} + V_{mpp}\left(\frac{\partial I}{\partial V}\right)_{mpp} = 0 \qquad (2)$$

The mathematical condition that the P&O algorithm iteratively approaches perturbing the converter duty cycle and monitoring the ensuing power change at each stage—is defined by equation (2). The degree to which the I–V characteristic approaches an ideal rectangle is measured by the fill factor $FF = P_{mpp} / (V_{oc}\ I_{sc})$; for premium monocrystalline silicon modules, FF usually surpasses 0.78.

Temperature Dependence and Compensation

Because $I_0 \propto T^3 \exp(-E_g / k_B\, T)$, the open-circuit voltage V_{oc} falls at roughly –83 mV °C^{-1} for a typical 36-cell, 12 V module (Skoplaki & Palyvos, 2009). Panel backsheet temperatures can exceed 52–60 °C under Nigerian insolation, significantly reducing the output power available (Skoplaki & Palyvos, 2009). The silicon V_{oc} temperature coefficient is used by the controller firmware to directly adjust the absorption and float charging voltage thresholds by –3 mV °C^{-1} per cell.

Hall-Effect Current Sensing

Measuring current in the 60 A power path demands galvanic isolation between the high-current rail and the digital control stage, and the Hall effect supplies exactly that. When a current-carrying conductor is placed in a perpendicular magnetic field B, charge carriers accumulate on one face of the conductor until the transverse electric field they establish precisely balances the magnetic force acting on them. At equilibrium the resulting Hall voltage is:

$$V_H = \frac{IB}{nqt} \qquad (3)$$

where t is the conductor thickness, n is the carrier density, and q is the elementary charge (Hart, 2011). The ACS712-50A provides intrinsic galvanic isolation between the power and signal domains by combining a precision Hall sensor and a copper current conductor on a single device. With a 2.5 V midpoint offset and a sensitivity of 40 mV A^{-1}, the entire 0–60 A measuring range maps comfortably into the Arduino's 0–5 V ADC input window without additional gain staging.

MATERIALS AND METHODS

System Design and Component Selection

Design Specifications

The following quantifiable goals were set before hardware was purchased: Maximum continuous output

current of 60 A; PV input voltage range of 12–100 V DC; nominal battery voltage of 12 V or 24 V (selectable); switching frequency of 20 kHz; P&O perturbation interval of 100 ms with a duty-cycle step ΔD = 0.5%; output voltage ripple below 1%; three-stage lead-acid charging profile consisting of Bulk, Absorption, and Float stages; and five separate hardware-plus-firmware protection mechanisms. These values are not arbitrary; each follows from a physical or device-level constraint. The lower limit of the PV input window is fixed by buck-converter operation itself: since $V_{out} = D\,V_{in}$ with $D < 1$, the array voltage must always exceed the battery terminal voltage plus the MOSFET and freewheeling-diode forward drops, so a 12 V floor is the smallest input that can still charge a 12 V bank. The upper limit is set jointly by the drain–source breakdown rating of the switching MOSFET, the reverse blocking rating of the freewheeling Schottky diode, and the division ratio of the sensing network, which must map the highest expected array voltage into the 0–5 V ADC window; the 100 kΩ/5.6 kΩ divider used here gives 1:18.9 and therefore saturates at approximately 95 V. The 20 kHz switching frequency is chosen to sit just above the upper limit of human hearing, eliminating audible magnetostrictive noise from the inductor, while remaining low enough that MOSFET switching losses stay small relative to the 28.8 W conduction loss and that the ATmega2560 can complete a full sense–compute–actuate cycle between perturbations. The 100 ms perturbation interval exceeds the LC network settling time by roughly an order of magnitude, ensuring each power measurement is taken at steady state rather than during a transient, and the 0.5% duty-cycle step is the smallest increment that produces a power change reliably distinguishable from ADC noise after 16× oversampling, thereby minimising steady-state oscillation about the MPP.

Buck Converter Design Equations

The asynchronous buck converter is the logical architecture of choice in situations when PV array voltage regularly surpasses battery voltage. Equations (4) to (7) below are the standard steady-state design relations for this topology and are quoted from Mohan et al. (2003) and Hart (2011) rather than derived here. The voltage conversion ratio at steady condition is:

$$V_{out} = D \times V_{in} \quad (4)$$

where D ($0 \leq D < 1$) is the PWM duty cycle, which the P&O algorithm continually modifies. The peak-to-peak ripple current standard (10% of I_{out} = 6 A) dictates the size of the inductor:

$$L = \frac{(V_{in} - V_{out}) \times D}{\Delta I_L \times f_s} \quad (5)$$

A 100 µH, 70 A rated toroidal core was chosen because substituting numbers for 48 V battery charging from a 72 V PV source at f_s = 20 kHz provides L ≈ 83 µH. To keep ripple below 1%, the minimum output capacitance needed is:

$$C_{out} \geq \frac{\Delta I_L}{8 \times f_S \times \Delta V_{out}} \quad (6)$$

A 4700 µF, 63 V low-ESR electrolytic capacitor was fitted in place of the calculated 781 µF minimum. The roughly six-fold margin was adopted because the calculated value guarantees the 1% ripple target only at the nominal operating point, whereas the delivered ripple degrades as load current rises and as electrolytic capacitance falls with age and temperature; the larger value also improves transient response when the charge controller steps between the bulk, absorption and float stages. The trade-off is a larger inrush current at switch-on, since the initial charging surge scales with capacitance. This was addressed by the 100 A input fuse, which is rated well above the measured surge, and by the soft-start behaviour inherent in the P&O algorithm, which begins each session at a low duty cycle and ramps upward in 0.5% steps rather than applying full duty instantaneously. No capacitor or MOSFET overheating attributable to inrush was observed during any of the switch-on cycles logged in this study. At rated current, the switching MOSFET's conduction power loss is:

$$P_{cond} = I^2 \times R_{DS(on)} \quad (7)$$

A typical aluminium heatsink can easily manage this degree of dissipation. All of the essential elements and the engineering justification for their choice are listed in Table 1.

Table 1: Key Component Specifications for the 60 A MPPT Charge Controller

Component	Model / Value	Key Parameter(s)	Engineering Justification
MOSFET Switch	IRF3205	V_{DS} = 55 V; I_D = 110 A; R_{DS}(on) = 8 mΩ	1.83× current derating; P_{cond} = 28.8 W at 60 A
Schottky Diode	MBR3045	45 V; 30 A; $V_o \approx 0.4$ V	Low conduction loss and quick recovery
Gate Driver	IR2110	Bootstrap; up to 600 V bus	High-side N-channel MOSFET drive
Buck Inductor	100 µH toroidal	70 A rated; 20 kHz	ΔI_l < 5% at full load
Output Capacitor	4700 µF / 63 V	ESR < 30 mΩ	ΔV < 1%; transient suppression
Current Sensor	ACS712-50A	40 mV A^{-1}; Hall-effect; isolated	Galvanic isolation; 0–50 A linear
Voltage Divider	100 kΩ / 5.6 kΩ	Ratio 1:18.9	Maps 100 V PV rail to 5 V ADC

Microcontroller	Arduino Mega 2560	16 MHz; 10-bit ADC; 6× PWM	P&O FSM; multi-channel sensing
NTC Thermistor	10 kΩ NTC	β = 3950 K	T-compensated thresholds; OTP
Input Fuse	100 A blade	80 V DC rated	Hardware OCP backup
Blocking Diode	1N5822	3 A; 40 V; $V_o \approx 0.4$ V	Prevents reverse current at night

General System Architecture (Fig. 1)

Figure 1, which shows the power and control pathways from source to load, depicts the general design of the manufactured controller. The solar array supplies energy down the upper power channel to the Input Stage, where a 100 A fuse serves as the last hardware protection against overcurrent, a blocking Schottky diode stops reverse current, and transient-voltage suppression clamps absorb incoming voltage spikes. Power then enters the LC filter network, which reduces switching ripple before the conditioned output reaches the battery terminals, after passing through the MOSFET switching stage. Decision-making and measurement are handled via the lower control path. Two ACS712-50A Hall-effect transducers and resistive voltage dividers form the basis of a sensing block that continuously measures electrical conditions and transmits the results to the Arduino Mega 2560. In order to operate the P&O finite-state machine, the microcontroller computes duty-cycle adjustments in real time and produces the corresponding PWM output. The IR2110 bootstrap driver then conditions this output to reliably switch the power MOSFET. An NTC thermistor installed on the heatsink performs two functions: it feeds real-time temperature data back into the charging algorithm so that absorption and float voltage thresholds are continuously adjusted to reflect the temperature dependence of silicon V_o^c, and it initiates a thermal shutdown if temperatures rise too high. All five protective layers are combined in the dashed band at the bottom of the diagram. These levels work simultaneously and can disable the converter in a single switching cycle if a defect is detected.

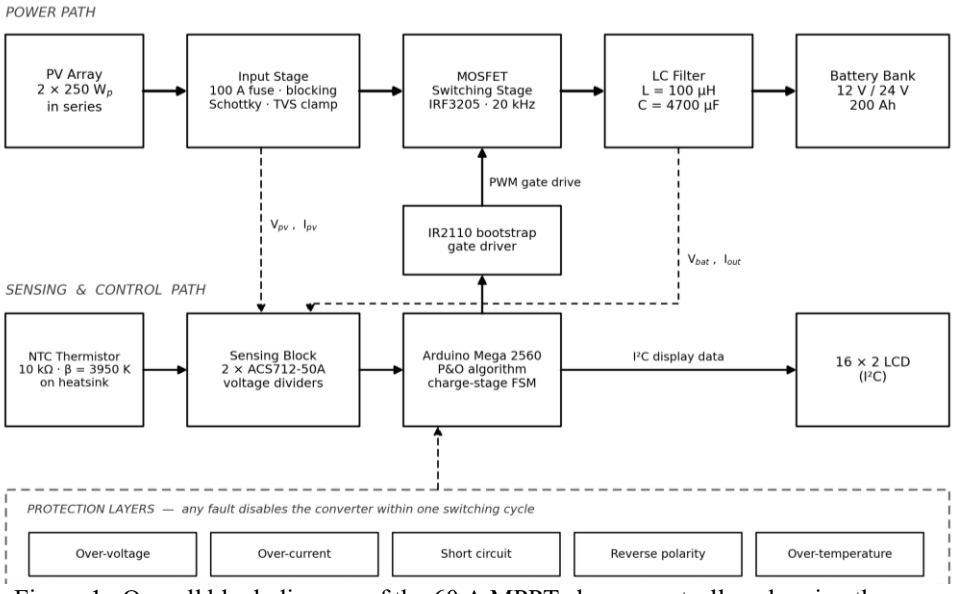

Figure 1: Overall block diagram of the 60 A MPPT charge controller, showing the power flow path (top) and the sensing, control, and protection signal paths (bottom).

Buck Converter Circuit Topology (Fig. 2)

Figure 2 shows the circuit of the buck converter stage. The PV array appears on the left as a current source whose terminal voltage V_{pv} is set by the instantaneous duty cycle. During the ON phase, transistor Q1 (IRF3205) conducts and current flows from the PV input, through inductor L, and into the battery while the inductor stores energy in its magnetic field. When Q1 turns off during the OFF phase, the collapsing field drives current through the freewheeling Schottky diode D1 (MBR3045), sustaining uninterrupted current delivery to the battery. The output capacitor C, connected in parallel with the battery, further filters the residual current ripple into a near-DC output voltage. The PWM gate signal produced by the IR2110 driver shown entering Q1's gate on the left is the signal the P&O algorithm modulates to steer the PV operating point towards the MPP. The conversion ratio $V_{out} = D \times V_{in}$ is noted at the base of the diagram for reference.

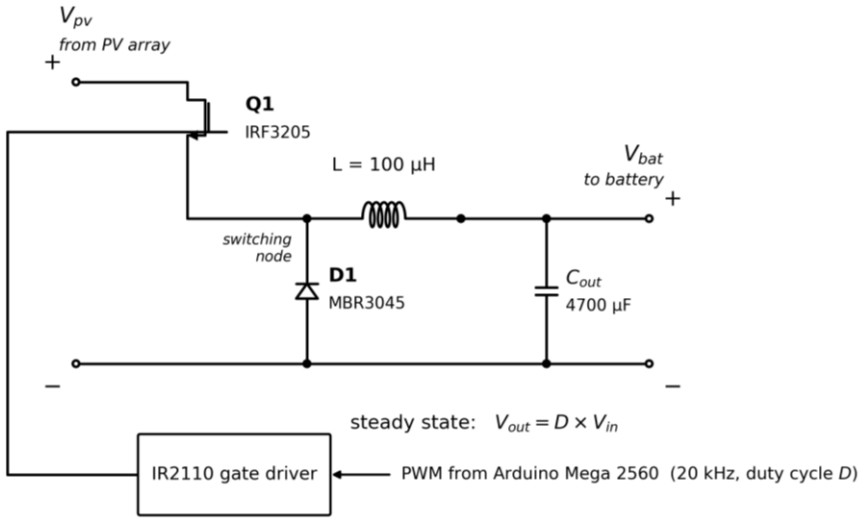

Figure 2: Asynchronous buck converter topology. Q1 (IRF3205) is the controlled switch; D1 (MBR3045) is the freewheeling Schottky diode; L = 100 µH; C = 4700 µF

P&O Algorithm and Embedded Firmware

Microcontroller and PWM Configuration

The Arduino Mega 2560 (ATmega2560, 16 MHz) was chosen for its six hardware PWM channels, 16-channel 10-bit ADC, and extensive open-source library support (Banzi & Shiloh, 2022). Timer 1 is configured in fast-PWM mode with ICR1 serving as the top value, producing an exact 20 kHz switching frequency:

$$f_{PWM} = \frac{f_{clk}}{N \times (1 + ICR1)} \quad (8)$$

The duty cycle is controlled by writing compare values to OCR1A over the range 0–799. A perturbation step of ΔD = 0.5% (four counts) was chosen to balance convergence speed against steady-state oscillation amplitude. Oversampling 16 successive ADC readings per channel effectively extends resolution from 10 to approximately 12 bits, sharpening the power discrimination between adjacent operating points.

Finite-State Machine

The firmware is structured as a four-state machine: SLEEP (nighttime, PV voltage below 10 V), BULK (full MPPT tracking at maximum current), ABSORPTION (constant-voltage regulation at 14.4 V for a 12 V bank, with natural current tapering until it drops below C/40 or after two hours), and FLOAT (maintenance charging at 13.6 V). In the BULK state the P&O loop executes every 100 ms. It reads V_{pv} and I_{pv}, computes the instantaneous power $P_k = V_{pv} I_{pv}$, and evaluates the power increment $\Delta P = P_k - P_{k-1}$. Depending on the sign of ΔP and on the sign of the preceding duty-cycle perturbation ΔD, the loop then increments or decrements OCR1A by four counts, so that the operating point migrates towards the condition dP/dV = 0 defined by equation (2).

Sensing and Control Architecture (Fig. 3)

The measurement signal chain from each physical quantity to the microcontroller output is shown in Figure 3. The system acquires four signals PV voltage, PV current, battery voltage, and output current each through a dedicated conditioning path. Voltage signals are scaled from their respective high-voltage rails down to the 0–5 V ADC window by resistive dividers, while current signals pass through ACS712-50A Hall-effect sensors whose galvanically isolated outputs are filtered by a first-order RC low-pass network (corner frequency 1.6 kHz) to attenuate switching-frequency noise ahead of the ADC pins. All four conditioned signals enter the Arduino Mega 2560, which computes instantaneous PV power, runs the P&O algorithm, manages charging-stage transitions, and generates three output signals: the PWM duty-cycle word directed to the IR2110 gate driver, the OCR1A register value encoding the precise switching period, and the I²C data stream supplying the 16×2 LCD display with real-time operating data. The complete sensing–computation–actuation cycle completes within 100 ms on each perturbation interval.

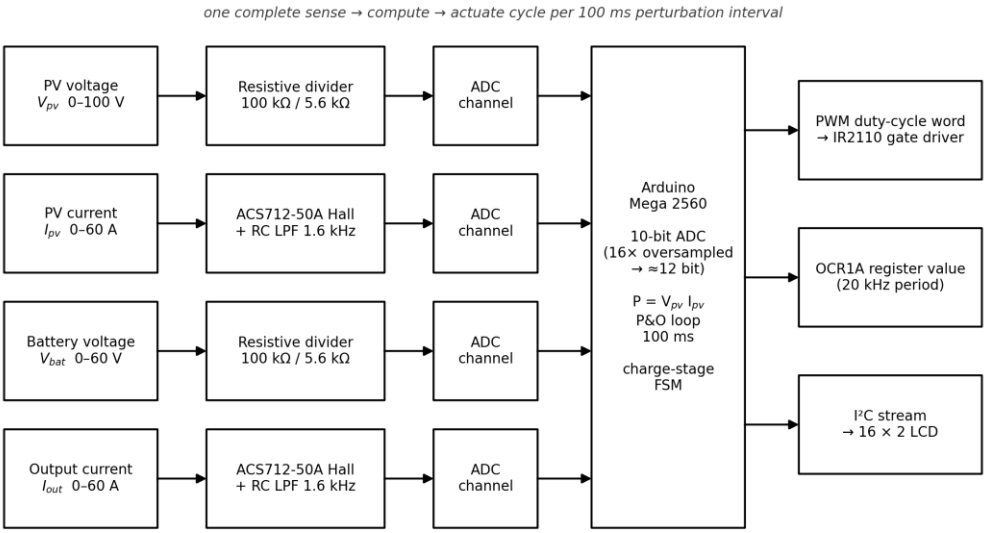

Figure 3: Sensing and control block diagram. Signal flow runs left to right from physical sensors through conditioning circuitry, ADC inputs, the Arduino Mega 2560 P&O processor, and finally to the gate driver, PWM output, and LCD display

Protection Architecture (fig. 4)

The five protective methods are arranged in a three-column arrangement in Figure 4, which displays each one's defect detection, logic, and system response. A hardware LM393 comparator continually monitors the PV rail for over-voltage protection, and if the voltage over 105 V, it pulls the IR2110 shutdown pin low within one switching cycle. Firmware adds a software check every 10 ms as a secondary layer. Over-current protection is handled primarily in firmware: when the measured output current exceeds 60 A on three consecutive samples (300 ms), the duty-cycle register is zeroed and switching ceases. The 100 A blade fuse serves as the hardware backstop should that firmware path fail. Hardware alone provides short-circuit safety; the fast-blow fuse blows before the firmware can react. In order to prevent erroneous current from reaching the control electronics, reverse-polarity protection uses an IRF9540N P-channel MOSFET inserted in the PV input line. Its gate-bias network maintains the device conducting under the proper polarity and cuts it off promptly upon reversal. Lastly, on each P&O cycle, over-temperature protection samples the heatsink NTC thermistor, linearly derating output current at one ampere per degree above 75 °C and completely shutting down at 85 °C. It only automatically resumes when the heatsink drops down below 65 °C.

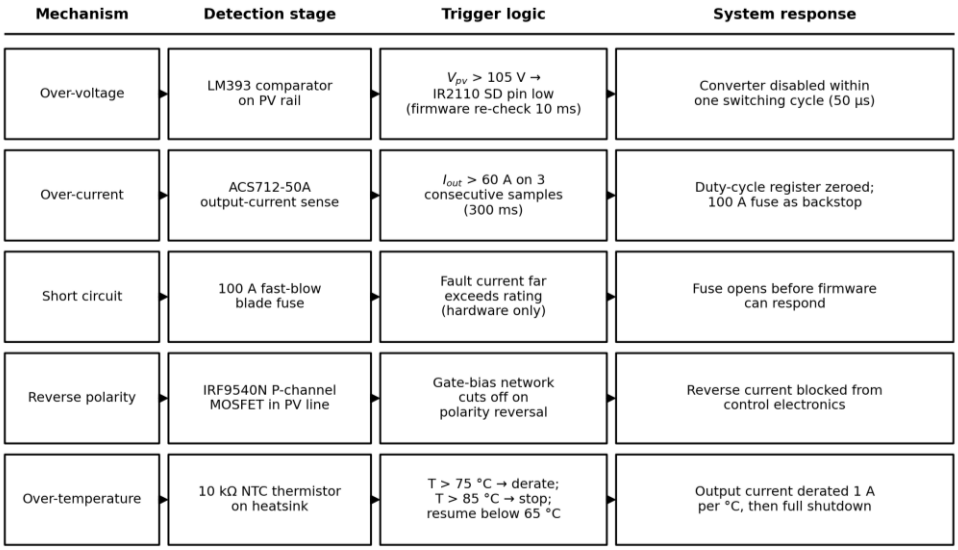

Figure 4: Protection circuit block diagram. Each row is one protection mechanism; columns show the detection stage, the trigger logic, and the system response

Experimental Methods

Laboratory Setup

A Keysight N5770A programmable DC power supply (0–150 V, 0–20 A) that functioned as a PV array emulator was used for laboratory characterisation. I–V characteristic datasets for a 250 Wp monocrystalline silicon panel were programmed at irradiance levels G = {200, 400, 600, 800, 1000} W m^{-2} and cell temperatures of 25 °C and 45 °C. The charge load consisted of a 12 V; 200 Ah flooded lead-acid battery bank. Once steady-state MPPT convergence had been reached (typically within 10 s of each irradiance step), input power $P_{in} = V_{pv}\, I_{pv}$ and output power $P_{out} = V_{bat}\, I_{out}$ were recorded simultaneously over 5-minute windows, with the procedure repeated three times per test condition.

Outdoor Setup

Outdoor evaluation was carried out on the roof of the Physics Building at FUTA over five consecutive clear-sky dry-season days (08:00–17:00 WAT). Two 250 W_p monocrystalline panels wired in series (combined 500 W_p; V_o^c = 75 V) charged a 24 V, 200 Ah battery bank. All electrical parameters were logged at one-minute intervals via an SD card shield mounted on the Arduino Mega. Solar irradiance was measured with an Apogee SP-110 pyranometer, while panel backsheet and ambient temperatures were recorded using K-type thermocouples connected to an Extech 421509 datalogger. MOSFET junction temperature was profiled with a FLIR E6 infrared camera.

MPPT tracking efficiency and power conversion efficiency were calculated as follows:

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% \qquad (9)$$

A complete list of the instruments utilised and their measurement ranges is given in Table 2.

Table 2: Measured Parameters, Instruments, and Measurement Ranges

Parameter	Instrument	Range / Resolution
PV voltage V_pv	Fluke 87V digital multimeter	0–1000 V DC / 0.1 V
PV current I_pv	Fluke 376 FC clamp meter	0–600 A AC/DC / 0.1 A
Output charge voltage	Fluke 87V digital multimeter	0–60 V DC / 0.01 V
Output charge current	Fluke 376 FC clamp meter	0–100 A DC / 0.1 A
Solar irradiance G	Apogee SP-110 pyranometer	0–2000 W m^{-2} / 1 W m^{-2}
Ambient temperature	K-type thermocouple (Extech 421509)	0–100 °C / 0.1 °C
MOSFET junction T	FLIR E6 infrared thermal camera	–20 to 250 °C / 0.1 °C
PWM duty cycle	Hantek 6022BE oscilloscope	0–100% / 0.1%
Output voltage ripple	Hantek 6022BE oscilloscope	mV AC / 1 mV

RESULTS AND DISCUSSION

Power Conversion Efficiency

Table 3 presents the findings of laboratory power conversion. The controller maintained η > 95.0% at all tested irradiance levels, peaking at 95.8% at G = 600 W m^{-2}. Equation (7) describes the quadratic relationship of MOSFET conduction loss on drain current, which is consistent with the little decrease to 94.4% for G = 800 W m^{-2}. Higher photocurrent amplitudes are associated with an increased ADC signal-to-noise ratio, which explains the partial recovery to 95.7% at G = 1000 W m^{-2}.

Table 3: Laboratory Power Conversion Results (12 V Battery Bank)

G (W m^{-2})	V_{pv} (V)	I_{pv} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	η (%)
200	38.4	2.1	80.6	13.2	5.8	76.6	95.0
400	39.1	4.3	168.1	13.5	11.9	160.7	95.6
600	40.2	6.2	249.2	13.8	17.3	238.7	95.8
800	41.0	8.5	348.5	14.0	23.5	329.0	94.4
1000	42.3	10.7	452.6	14.4	30.1	433.4	95.7

MPPT Tracking Efficiency

Pmpp was obtained from the internal I-V model of the emulator, and MPPT tracking efficiency is shown in Table IV. The P&O algorithm maintained ηMPPT ≥ 96.4% in every test scenario. There is a well-established physical explanation for the reduction at G = 200 W m^{-2}: at low irradiance, the P–V characteristic becomes noticeably flatter, reducing the power differential between adjacent duty-cycle steps and enabling the tracker to oscillate more widely around the true MPP. This low-irradiance tracking error could be decreased by using an adaptive step-size variant of the P&O algorithm, but doing so would increase firmware complexity.

Table 4: MPPT Tracking Efficiency vs. Irradiance

G (W m^{-2})	P_{mpp} (W)	P_{extr} (W)	η_{MPPT} (%)
200	79.5	76.6	96.4
400	165.0	160.7	97.4
600	243.0	238.7	98.2
800	337.0	329.0	97.6
1000	442.0	433.4	98.1

Thermal Performance

The MOSFET junction and heatsink temperatures as a function of load current are displayed in Table V, in which I_{load} is the steady output current delivered to the battery, T_{MOSFET} is the MOSFET junction temperature obtained by infrared thermography of the device package, $T_{heatsink}$ is the temperature measured at the heatsink base directly beneath the MOSFET mounting point, and P_{cond} is the conduction loss calculated from equation (7) using the room-temperature datasheet value of R_{DS}(on). Each row is the mean of three measurements taken after 15 minutes at the stated current, by which point the thermal transient had settled to within 1 °C. The junction temperature reached 76 °C at the rated 60 A, well below the IRF3205 absolute maximum of 150 °C. The thermal design is validated because the derived junction-to-ambient thermal resistance $\Psi ja = (76 – 28) / 28.8 \approx 1.67$ °C W^{-1} matches the datasheet specification for the chosen heatsink. The system was thermally stable during all test periods and the 85 °C shutdown threshold was never achieved, despite the fact that phonon scattering causes R_{Ds}(on) to increase with temperature (carrier mobility $\mu_n \propto T^{-2\cdot4}$), elevating effective conduction loss by about 35% at 76 °C relative to the 25 °C datasheet value.

Table 5: Thermal Efficiency against Load Current

I_{load} (A)	T_{MOSFET} (°C)	T*h*^{e}ɐ$^{t}_{s}$^{In}□ (°C)	P$^{c}_{o}$nd calc. (W)
10	34	30	0.8
20	42	37	3.2
30	51	45	7.2
40	60	53	12.8
50	69	61	20.0
60	76	68	28.8

Outdoor Performance

The controller produced an average conversion efficiency of ηavg = 94.8% and an average MPPT tracking efficiency of $\eta MPPT,avg$ = 97.5% over the five clear-sky test days under naturally changing irradiance ranging from 150 to 980 W m^{-2} per day. There were no protection faults at any time, and transitions between the bulk, absorption, and float charge stages were smooth. The temperature-compensation firmware precisely tracked the silicon V_{oc} temperature coefficient and prevented battery overcharging by lowering the absorption voltage setpoint by 210–270 mV in response to panel backsheet temperatures of 52–58 °C. Elevated panel temperatures, naturally fluctuating irradiance that increases instantaneous P&O tracking error, and cable resistance losses that were not present in the laboratory configuration all contribute to the slight discrepancy between peak laboratory efficiency (95.8%) and average outdoor efficiency (94.8%).

Comparison with Related Work

The current design's rating of 60 A is higher than that of the majority of locally documented MPPT controllers in Nigeria, which normally don't go over 30 A (Okonkwo & Ezechukwu, 2023). The obtained ηMPPT of 98.2% is similar to the 98.1% reported by ARM Cortex-M4 implementations (Huynh & Dunnigan, 2016), however, the platform cost is significantly higher. Using Fuzzy Logic Control on an STM32 at 40 A, Verma *et al.* (Verma et al., 2016) achieved 98.7%, however, they observed significantly higher parameter-tuning complexity. When combined, these studies indicate that low-cost, open-source microcontroller platforms can achieve comparable MPPT performance, significantly reducing the manufacturing barrier for off-grid solar systems in environments with limited resources.

CONCLUSION

The present work describes a 60 A MPPT charge controller which is physically fabricated and fully characterised in the laboratory as well as outdoors using the principles of semiconductor physics. Throughout the project, the design choices were all motivated by direct physical foundations: the use of the Hall effect for galvanically isolated current sensing, the phonon-scattering-limited temperature dependence of on-resistance in MOSFETs, and the nonlinear transport characteristics of silicon p-n junctions.

Peak MPPT tracking efficiency was 98.2%, peak power conversion efficiency was 95.8%, the output voltage

ripple was 0.67%, and the maximum MOSFET junction temperature was 76 °C at the rated 60 A load in the lab. Across the five days of the good weather, average outside efficiencies of 94.8% and 97.5% were maintained, with no protection issues reported. All these results show that high-performance MPPT charge controllers can be manufactured locally using the commercially available semiconductor components at a performance comparable to the commercially available controllers. This directly impacts the availability of PV electricity in sub-Saharan countries.

Future work will explore an adaptive step-size P&O variation to improve tracking precision at low light intensities, synchronous rectification to reduce losses associated with the conduction of the freewheeling diode and integration of an ESP32 Wi-Fi module for remote monitoring and problem diagnosis.

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