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Optimizing Quantum-dot Cellular Automata Circuits for Nano communication: A Reversible Hamming Code Implementation

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ABSTRACT

Quantum-dot cellular automata (QCA) is a transistor-free computing paradigm that allows the realisation of quicker, denser, and more energy-efficient nanoscale circuits. When compared to traditional complementary metal-oxide-semiconductor (CMOS) circuits. Its tiny size along with low power dissipation are some of its advantages in reversible logic. A major concern is the high cell count required for the implementation of these circuits, which hinders energy and area optimisation. This study suggests a concept of a 58-cell low-power HCG circuit that uses a reversible Feynman gate to process three-bit data. Using six-bit message signals, an error detector parity bit (EDP) circuit for Hamming code was implemented using 88 cells. To make sure the circuit functions correctly, Quantum Dot Cellular Automata Designer simulator version 2.0.3 is used to verify the proposed circuits, and QCA Designer-E is utilised to analyse the circuits' energy dissipation. According to the simulation results, the suggested HCG circuits require 50% less area and 20.5% fewer cells. The EDP circuit further enhances the area occupied by 20.7% and the number of cells by 50%. The outcome also demonstrates that the suggested circuit's energy dissipation rises with the number of cells. As a result of this, the suggested reversible QCA design shows enhanced performance and emphasises the applicability of QCA for upcoming high-density and energy-efficient nanoscale communication systems.

Keywords:
Area optimisation,
Energy dissipation,
Error detection parity,
Nanoscale communication systems,
Reversible logic.

INTRODUCTION

The demand for expandable transistor size and reduced power usage in electronic circuits has spurred research into energy- and space-efficient technologies. Power loss at the contacts of ballistic transistors is inevitable with modern CMOS silicon technology (Kalpana et al., 2024; Yang et al., 2008). Very high-scale integration has led to a progressive reduction in the size of CMOS devices, but this method's limitations have already been reached (Huang et al., 2021; Kumar & Sasamal, 2017). As CMOS devices continue to shrink, numerous short-channel effects (SCEs) must be addressed in addition to higher power usage and leakage.

CMOS replacements are crucial for preserving circuit shrinking and improving microprocessor efficiency (Das & De, 2017; Gassoumi et al., 2019; Sharma, 2021). Quantum-dot cellular automata (QCA) is considered one of the most viable substitute that deals with speed, power, and size difficulties. Binary values are encoded by QCA using the magnetization or charge configuration of its cells, and the data is processed using intercellular coupling mechanisms (Lu et al., 2013; Norouzi & Heikalabad, 2019; Tougaw & Khatun, 2013). High density of device, quick speed of clock, and incredibly minimal consumption of power are features of non-transistor quantum-dot cellular automata technology (Das & De, 2016, 2017; Tougaw & Khatun, 2013). Binary information is encoded by the mutual interactions between electrons in the cells, which impact their charge configurations or magnetization states. This interaction forms the basis for information flow and other calculations (Roohi et al., 2014; Singh et al., 2016). Due to its efficiency, which enables faster data transmission rates, QCA is appropriate for high-speed data transfer applications (Aondofa et al., 2026).

Quantum cellular automata and reversible computing were suggested by Landauer (Rolf Landauer, 1961) as a solution to the issues of size, speed, and power consumption. An intriguing design strategy is reversible logic that generates no heat per byte of data loss and is

thus extremely energy-efficient (Kaity & Singh, 2021). The energy loss in an irreversible circuit is quantitatively equivalent to kTln 2 J for each bit of information translation (Bennett, 1973).

Noise and other environmental disruptions in digital communication lead to errors throughout the data transfer process from source to destination (Kavitha, 2018; Sengupta et al., 2019). An error occurs when a single bit is altered during transmission. Error detection and repair circuits are an element of every digital circuit to lessen these issues (Sengupta et al., 2019). A reversible implementation of a Hamming encoder and decoder is presented in (Kavitha, 2018). The Xilinx ISE 14.4 design suite is used to obtain the simulation results. The simulation results offer a novel approach to lower power consumption in conventional Hamming code circuits by integrating reversible logic gates. 18 garbage outputs, 27 gates, 39 quantum cost, and 1 ns latency. The Hamming code converter, decoder, and corrector unit were enhanced and made reversible in (Xie et al., 2023); 18-gate and 18-quantum-cost designs were implemented using a Toffoli netlist. The outcome demonstrated that the proposed designs might prove to be essential components of future quantum architectural designs. In (Kaity & Singh, 2021), a highly dependable, reversible, and area-efficient Hamming generator, detector, and corrector circuit is presented; the generator and corrector circuits have no garbage values and an exceptional area efficacy of 29.5%. In a distinct study (Shan & Zhoe, 2020), a 3-input XOR gate and basic cells are employed to create and implement a new 3-to-8 decoder. These parts are used to construct an electronic circuit that implements Hamming codes and incorporates the QCA-based technique.The proposed network for hamming communication has shown a notable decrease in consumed cells (54.27%) and an improvement in occupied area (10.14%).

A channel communication system based on VHDL was created in (Muneeb & Namratha, 2022)incorporating channel coding and decoding elements into the entire architecture. The findings indicate that the system's ability to repair errors can be improved and its high rate of bit error can be considerably reduced while being transmitted in high-bit-rate circumstances. However, with these advancements, developing an energy-efficient system that provides decreased energy loss, fast operation, and effective use of available space is crucial since power consumption and area occupancy are essential aspects in circuit design.

This study focuses on creating a reversible QCA-based Hamming code generator and an error detector circuit for three-bit message processing. QCADesigner-E finds energy dissipation, and QCADesigner version 2.0.3 verifies the designs. The performance characteristics that are taken into account are cell count, clock delay, occupied area, and energy consumption.

Basic Theory

Reversible logic gates are computational elements that preserve an equal number of input and output variables by uniquely matching each input pattern to a single output pattern (Abdessaied & Drechsler, 2016; Soeken et al., 2015). For every input vector arrangement, a distinct output vector pattern is generated (Biswas et al., 2014). This feature reduces power usage by preventing information loss. Reversible logic does not allow for feedback loops or fan-outs. Reversible logic circuits have few input constants, few reversible gates, and few garbage outputs. Subsequently, each cell in quantum-dot cellular automata, a cell-based array structure, comprises four quantum dots arranged at the vertices of a square (Mehta & Dhare, 2017).The majority of the electric charge in the cell is stored in these dots. Additionally, tunneling between the dots is possible for two electrons motion. Electrons cannot tunnel out of a cell because of probable obstacles between cells. Because of Coulombic repulsion, which controls electron interaction, electrons must occupy diagonal opposing locations in order to be stable. A typical QCA cell with four numbered quantum dots (sites), is shown in Figure 1(a). The cell's polarization (P) which defines its logical state, is computed using (Lent & Tougaw, 1993)

$$P = \frac{(\rho_1+\rho_3)-(\rho_2+\rho_4)}{\rho_1+\rho_2+\rho_3+\rho_2} \quad (1)$$

Where $\rho_1, \rho_2, \rho_3, \rho_4$ are electron probabilities in the cell's four quantum dots.

The ground state eigen function (ρ_i), is given by

$$\rho_i = \langle \Psi_o | \hat{\eta}_i | \Psi_o \rangle \quad (2)$$

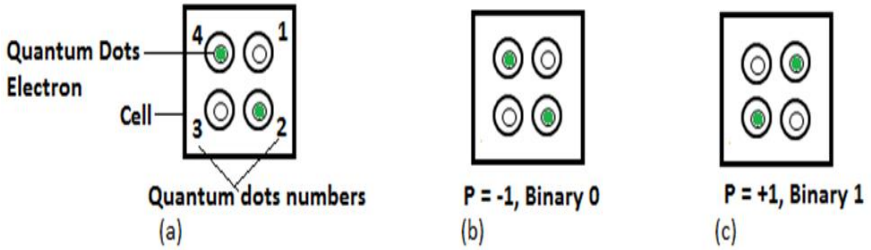

Figure 1: QCA (a) cell architecture (b) polarization P = "-1" (c) P = "+1". (Mehta & Dhare, 2017)

The cell's ground energy state is given by $|\Psi_o\rangle$ and is defined by

$$|\Psi_o\rangle = \sum_j \Psi_j^0 |\phi_j\rangle \quad (3)$$

Where Ψ_j^o is the coefficient of the corresponding basis vector, as as ascertained by directly diagonalizing the Hamiltonian, and $|\phi_j\rangle$ is the jth basis vector. When electrons are placed as shown in Figure 1(b), the cell displays a polarisation value of P=−1, which Equation (1) interprets as binary 0 (Logic 0). On the other hand, the electron configuration depicted in Figure 1(c) results in a cell polarisation of P=+1, which is binary 1 (Logic 1). When cell j's polarisation coincides with that of cell i, cell i serves as the driving cell in a two-cell configuration made up of cells i and j. The associated two-state model is evaluated using the Hamiltonian for a single cell i in an N-cell configuration (Walus et al., 2004).

$$\hat{H} = \begin{bmatrix} -\frac{1}{2}P_j E_{i,j}^k & -\gamma_j \\ -\gamma_j & \frac{1}{2}P_j E_{i,j}^k \end{bmatrix} \quad (4)$$

Where P_j denotes the polarisation related to cell j, $E_{i,j}^k$ is the kink energy and γ_i is the tunnelling energy. The kink energy, E_kink, can be used to quantify the Coulombic interaction between two cells expressed as the difference between the electrostatic energies of cells that are equally polarised and those that are oppositely polarised (Snider et al., 1999).

$$E_{kink}^{i,j} = E_{opposite}^{i,j} - E_{same}^{i,j} \quad (5)$$

$E_{opposite}^{i,j}$ Is the expression for the interaction energy of cells i and j with opposite polarisations, while $E_{same}^{i,j}$ is the expression for the interaction energy when both cells have the same polarisation. The energy of the electrostatic interaction between two cells is used to calculate the state energy. Equation (6) is used to determine the electrostatic energy related to cells i and j.

$$E^{i,j} = \frac{1}{4\pi\varepsilon_O\varepsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{q_n^i q_m^j}{|r_n^i - r_m^j|} \quad (6)$$

where ε_o is the permittivity of free space, ε_r is the relative permittivity of the medium, q_i^n is the charge at dot n of cell i, q_m^j is the charge at dot m of cell j, The positions of the corresponding dots are indicated by the vectors r_n^i and r_m^j, and the distance between them is indicated by $|r_n^i - r_m^j|$

MATERIALS AND METHODS

The Hamming coding technique is utilized for generating, detecting, and correcting three-bit data. The Feynman gate is used to create parity values, calculate the necessary amount of parity bits, locate them inside the message signal, and arrange the data and parity bits into the proper encoding structure. Additionally, the created Hamming code is used to demonstrate the designs of the error bit position detector and bit correction circuits. The number of parity bits needed to generate a Hamming code for a given data length is determined using

$$2^P \geq D + P + 1 \quad (7)$$

Where D is the amount of data bits and P is the required number of parity bits.

The Feynman reversible gate, that has two inputs and two outputs, is used in the circuit that generates parity bits as suggested in (Galadima et al., 2023). One output produces the exclusive OR (XOR) of both input values, while the other output directly reflects the first input. The block diagram and QCA layout of the Feynman gate are illustrated in Figures 2a and b.

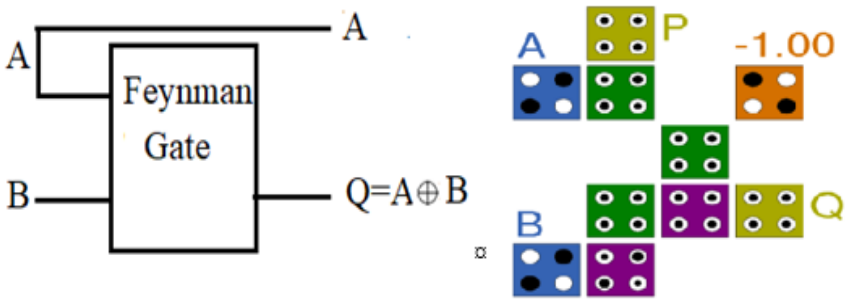

Figure 2: (a) Logic diagram of the proposed Feynman gate (b) The corresponding QCA design

Hamming (6, 3) Code

There are three data bits and three parity bits in the Hamming (6, 3) coding. The HCG relation in equation (7) determines the number of parity bits. Table 1 illustrates the proper bit configuration.

Table 1: Hamming Code Bit Positions

Bit position	1	2	3	4	5	6
Parity/Data bit	P1	P2	P3	P4	P5	P6

$P1 = D1 \oplus D2$ (8)
$P2 = D1 \oplus D3$ (9)
$P3 = D2 \oplus D3$ (10)

The data bits at locations 3 and 5 are checked by parity bit 1 (P1). Parity bit 2 (P2) confirms the data bits at positions 3 and 6, while parity bit 4 (P3) verifies the data bits at positions 5 and 6. Figures 3a and b display the block diagram and QCA configuration for the Hamming (6, 3) code generator. Three Feynman reversible gates are utilized in the design of this circuit. Each gate receives two data bits as input and outputs one data bit and one parity bit.

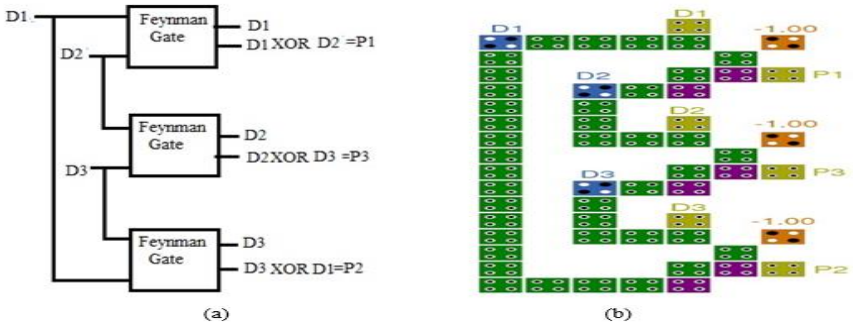

Figure 3: Proposed reversible Hamming (6, 3) code generator circuit (a) Logic diagram (b) QCA layout

As a result, we receive all of the message bits, including data and parity bits message at the circuit's output. Equations (11), (12), and (13) show the expressions to produce the EDP bits.

$EDPI = P1 \oplus D1 \oplus D2$ (11)
$DP2 = P2 \oplus D1 \oplus D3$ (12)
$EDP3 = P3 \oplus D2 \oplus D3$ (13)

Figures 4a and b depict the block diagram and QCA configuration for the circuit needed to produce the EDP bits from the message bits in the Hamming (6, 3) error detection system. For this, six Feynman reversible gates are required, as depicted in Figure 4. These gates use the input data bits and parity bits to create the EDP bits.

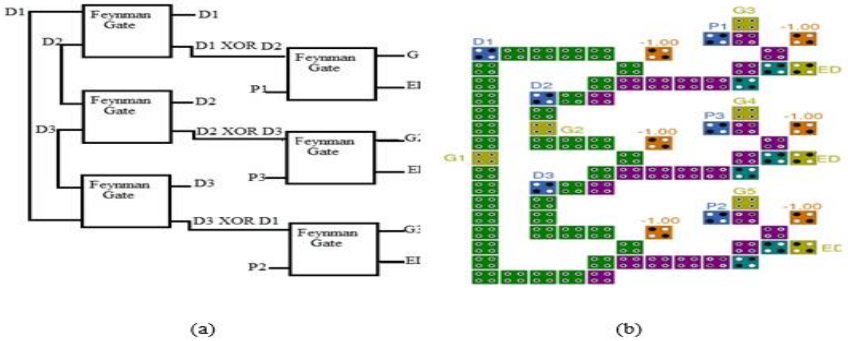

Figure 4: Proposed reversible Hamming (6, 3) error detector circuit (a) Logic diagram (b) QCA layout

RESULTS AND DISCUSSION

The simulation results produced by the Hamming (6, 3) code generator circuits are presented and discussed in this section. Additionally, it addresses six-bit message error detector circuits for hamming codes. The QCA-Designer tool version 2.0.3 is used to design and validate the suggested circuit (Walus et al., 2004). The default simulation parameters are: Quantum dot diameter = 5 nm, QCA cell size = 18 nm, sample count = 50,000, and convergence tolerance = 0.001, radius of effect = 65 nm relative permittivity = 12.9, $clocklow = 3.8E^{-23}J$, $clockhigh = 9.8E^{-22}J$, clock amplitude factor = 2.000, layer separation = 11.5 nm and maximum iterations per sample = 100.

Simulation Result of the Hamming (6, 3) Code

Figure 5a displays the (6, 3) Hamming generator circuit's input/output waveforms. The simulation results are tested with equations (8), (9) and (10). For inputs D1=0, D2=0, and D3=0, the outputs are P1=0, P2=0, AND P3=0. The output are P1=0, P2=1, and P3=1 when the input values are D1=0, D2=0, and D3=1, and the process continues. Therefore the circuit functions efficiently. Compared to the structure of (Kaity & Singh, 2021), the suggested

(6,3) Hamming code generator has 58 cells, a 20.54% reduction. Furthermore, the suggested (6,3) Hamming code generator structure's occupied area is 0.04 μm^2, which results in a 50% improvement over the (Kaity & Singh, 2021) structure.

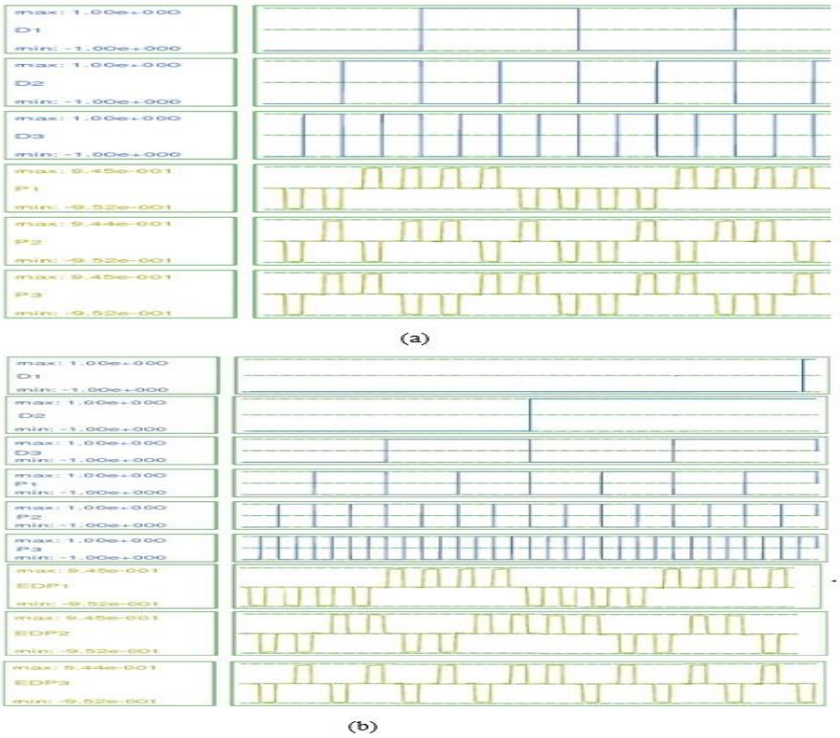

Figure 5: Input/output waveforms of the reversible Hamming (6,3) code (a)generator circuit (b) code error detector circuit

The input/output waveforms in Figure 5b demonstrates the generation of the EDPs from the message signal. The results of the simulation show that when the Inputs is D1= 0, D2= 0 and D3= 0, the Output is P1= 0, P2=0 and P3=0. Similarly, when the Inputs are D1= 0, D2= 0 and D3=1, Output becomes P1= 0 P2=1 and P3=1, and the procedure is repeated; these outcomes are consistent with equations (11), (12), and (13) for other input data values. In comparison to the design of (Kaity & Singh, 2021), the suggested (6,3) error detector circuit contains 88 cells, a 20.72% reduction. A further improvement of 50% over the (Kaity & Singh, 2021) structure is achieved by the occupied area of the suggested Hamming code generator error detector circuit structure, which is 0.08 μm^2.
Table 2 summarizes the key findings of this study in relation to prior research based on the number of cells, occupied area, and delay

Table 2: Summary of the Key Findings of This Study in Relation with Previous Work

QCA circuit	This work			Kaity & Singh, (2021)		
	Cell count	Total area (μm^2)	Latency (ns)	Cell count	Total area (μm^2)	Latency (ns)
Hamming (6,3) code generator	58	0.047	0.5	73	0.08	0.5
Hamming(6,3) code error detector	88	0.086	0.75	111	0.16	0.75

Energy dissipation

The energy dissipation of the suggested circuits is computed using QCA Designer-E version 2.2, an improved version of QCA Designer. The average and total energy for each of the proposed circuits are calculated, shown, and compared with previous research in Table 3. It is observed that energy dissipation increases along with the number of cells.

Table 3: Comparison of this Work's Energy Dissipation with Other Works

QCA circuit	This work		Kaity & Singh, (2021)	
	Total energy dissipation(eV)	Average energy dissipation (eV)	Total energy dissipation(eV)	Average energy dissipation (eV)
Hamming (6,3) code generator	1.92×10^{-2}	1.74×10^{-3}	4.11×10^{-2}	3.73×10^{-3}
Hamming(6,3) code error detector	3.00×10^{-2}	2.73×10^{-3}	7.79×10^{-2}	7.09×10^{-3}

CONCLUSION

In this study, circuits to generate three-bit error-detecting codes were developed. Additionally, it covers circuit design for error detectors for six-bit messages. To develop these circuits, we utilize the coplanar crossover method and 2 × 2 Feynman reversible gates. Here, we decrease the area required for the circuits by using the Feynman gate having the least cells. The coplanar crossover makes these circuits more feasible because just one layer is required to create them. The proposed circuit for the Hamming code exhibits significant gains in clock delay performance, cell count efficiency, and area utilization. The design HCG circuits have reduced space usage by at least 50% and the number of cells needed by 20.54%. Compared to the recently suggested circuit, the EDP circuit has an outstanding 50% reduction in occupied area and 20.72% fewer cells. Furthermore, the circuits exhibit outstanding energy efficiency, with a maximum energy dissipation of 3.00×10-2 eV for the recommended designs and an extremely low energy dissipation of 1.92×10-2 eV. Further research may focus on improving latency, energy consumption, and fault tolerance to increase the viability and flexibility of circuits based on QCA for demanding computing needs. By expanding on the groundwork established by this study, researchers can keep coming up with new ideas and solutions to meet the ever-growing demands of present-day communication networks.

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